INTEGRATING A POWER ARBITER IN A PROCESSOR

FIELD OF THE INVENTION

[0001] Embodiments relate to power management of a system, and more particularly to power management of a multicore processor.

BACKGROUND

[0002] Advances in semiconductor processing and logic design have permitted an increase in the amount of logic that may be present on integrated circuit devices. As a result, computer system configurations have evolved from a single or multiple integrated circuits in a system to multiple hardware threads, multiple cores, multiple devices, and/or complete systems on individual integrated circuits. Additionally, as the density of integrated circuits has grown, the power requirements for computing systems (from embedded systems to servers) have also escalated. Furthermore, software inefficiencies, and its requirements of hardware, have also caused an increase in computing device energy consumption. In fact, some studies indicate that computing devices consume a sizeable percentage of the entire electricity supply for a country, such as the United States of America. As a result, there is a vital need for energy efficiency and conservation associated with integrated circuits. These needs will increase as servers, desktop computers, notebooks, Ultrabooks™, tablets, mobile phones, processors, embedded systems, etc. become even more prevalent (from inclusion in the typical computer, automobiles, and televisions to biotechnology).

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. **1** is a block diagram of a portion of a system in accordance with an embodiment of the present invention.
[0004] FIG. **2** is a block diagram of a processor in accordance with an embodiment of the present invention.
[0005] FIG. **3** is a block diagram of a multi-domain processor in accordance with another embodiment of the present invention.
[0006] FIG. **4** is an embodiment of a processor including multiple cores.
[0007] FIG. **5** is a block diagram of a micro-architecture of a processor core in accordance with one embodiment of the present invention.
[0008] FIG. **6** is a block diagram of a micro-architecture of a processor core in accordance with another embodiment.
[0009] FIG. **7** is a block diagram of a micro-architecture of a processor core in accordance with yet another embodiment.
[0010] FIG. **8** is a block diagram of a micro-architecture of a processor core in accordance with a still further embodiment.
[0011] FIG. **9** is a block diagram of a processor in accordance with another embodiment of the present invention.
[0012] FIG. **10** is a block diagram of a representative SoC in accordance with an embodiment of the present invention.
[0013] FIG. **11** is a block diagram of another example SoC in accordance with an embodiment of the present invention.
[0014] FIG. **12** is a block diagram of an example system with which embodiments can be used.
[0015] FIG. **13** is a block diagram of another example system with which embodiments may be used.
[0016] FIG. **14** is a block diagram of a representative computer system.
[0017] FIG. **15** is a block diagram of a system in accordance with an embodiment of the present invention.
[0018] FIG. **16** is a block diagram illustrating an IP core development system used to manufacture an integrated circuit to perform operations according to an embodiment.
[0019] FIG. **17** is a block diagram of a portion of a system in accordance with an embodiment of the present invention.
[0020] FIG. **18**A is a block diagram of an example switch capacitor circuit in accordance with an embodiment of the present invention, in a first phase.
[0021] FIG. **18**B is a block diagram of an example switch capacitor circuit in accordance with an embodiment of the present invention, in a second phase.
[0022] FIG. **19** is a schematic diagram of a power delivery circuit in accordance with an embodiment of the present invention.
[0023] FIG. **20** is a flow diagram of a method in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0024] In various embodiments, greater power efficiency for an integrated circuit can be realized by providing one or more integrated voltage regulators that switchably couple charge to selected ones of multiple voltage rails of the integrated circuit. This switching may be based on a power arbitration scheme implemented by a power arbiter circuit which, in some embodiments, may be implemented within the integrated voltage regulator itself. As such, embodiments enable a high efficiency integrated voltage regulator (IVR) implementation having a power arbiter, which may be implemented integrally to the IVR, that provides an internal voltage regulator (VR) for low current power paths (also referred to as "rails").
[0025] Embodiments may enable a power delivery architecture having switched capacitor-based power benefits with reductions in external bill of materials (BOM) area and cost, on-die pin count, switching die area, and accurate control over different internal rails. Although the scope of the present invention is not limited in this regard, embodiments may be used in connection with processors or systems on chip (SoCs), and/or for on-board power management integrated circuit (PMIC) regulators for incorporation in cost and form-factor sensitive systems. Using an embodiment, a reduced number of switcher blocks may be present, realizing package size, BOM cost, power, and area benefits.
[0026] Although the following embodiments are described with reference to energy conservation and energy efficiency in specific integrated circuits, such as in computing platforms or processors, other embodiments are applicable to other types of integrated circuits and logic devices. Similar techniques and teachings of embodiments described herein may be applied to other types of circuits or semiconductor devices that may also benefit from better energy efficiency and energy conservation. For example, the disclosed embodiments are not limited to any particular type of computer systems. That is, disclosed embodiments can be used in many different system types, ranging from server computers (e.g., tower, rack, blade, micro-server and so forth), communications systems, storage systems, desktop computers of any configuration, laptop, notebook, and tablet computers (including 2:1 tablets, phablets and so forth), and may be also used in other devices, such as handheld devices,